AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A client-server semiconductor verification system, said system comprising:

a client computer storing a test job for testing a design of a programmable logic circuit, said test job having test vectors and configuration data for said programmable logic circuit;

a server coupled to said client computer by way of a network, said server receiving said test job from said client computer; and

a plurality of ~~system~~ systems under test coupled to said server ~~and~~, wherein each system under test of said plurality of systems under test has a different programmable logic device architecture and a selected system under test of said plurality of systems under test has a ~~having said~~ programmable logic circuit which is configured with a circuit design implemented according to said configuration data, said selected system under test receiving said test vectors and outputting result vectors to the client computer by way of said server.

2. (Previously Presented) The system of claim 1 wherein said client computer further has expected results.

3. (Previously Presented) The system of claim 2 wherein said client computer generates said test vectors.

4. (Previously Presented) The system of claim 3 wherein said client computer generates said expected results.

5. (Original) The system of claim 2 wherein said test vectors and said expected results are generated by an external device.

6. (Currently Amended) A client-server semiconductor verification system, said system comprising:

a plurality of client computers, wherein a client computer of said plurality generates a test job for testing the design of a programmable logic circuit and comprises test vectors and configuration data for said programmable logic circuit;

a server coupled to said plurality of client computers by way of a network, said server receiving said test job from said client computer; and

a plurality of systems ~~system~~ under test coupled to said server, wherein each [[said]] system under test of said plurality of systems under test has a different programmable logic device architecture, and wherein a selected system under test of said plurality of systems under test has ~~having said~~ a programmable logic circuit which is configured with a circuit design implemented according to [[said]] configuration data of a test job and ~~receiving~~ receives said test vectors of said test job and ~~outputting~~ outputs result vectors to the client computer by way of the server.

7. (Original) The system of claim 6 wherein said server comprises a network interface.

8. (Original) The system of claim 6 wherein said server comprises a system under test interface.

9. (Cancelled)

10. (Previously Presented) The system of claim 6 further comprising another server coupled to said plurality of client computers by way of the network.

11. (Currently Amended) A client-server semiconductor verification system, said system comprising:

a plurality of client computers, wherein a client computer of said plurality generates a test job for testing the design of a programmable logic circuit and has test vectors and configuration data for said programmable logic circuit;

a job distribution server coupled to said plurality of client computers by way of a network, said job distribution server receiving said test job from said client computer;

a server coupled to said plurality of client computers by way of said job distribution server, said server receiving said test job from said job distribution server; and

a system under test of a plurality of systems under test having different programmable logic device architectures, said system under test having programmable logic which is configured with a circuit according to said configuration data of said test job coupled to said system under test and being coupled to said server, wherein said system under test receives ~~receiving~~ said test vectors and ~~outputting~~ outputs result vectors to said client computer by way of said server and said job distribution server.

12. (Previously Presented) The system of claim 11 further comprising a plurality of servers coupled to said plurality of client computers by way of said job distribution server.

13. (Original) The system of claim 12 wherein said plurality of servers are coupled to said job distribution server by way of a second network.

14. (Cancelled)

15. (Currently Amended) The system of claim [[14]] 13 wherein each system under test of said plurality of systems under test is coupled to a server of said plurality of servers.

16. (Currently Amended) A method of verifying a semiconductor design by way of a server, said method comprising the steps of:

storing a test job for testing a design of a circuit in a client computer, said test job having test vectors and configuration data for a circuit implemented in

programmable logic;

providing a plurality of systems under test, each system under test having a different programmable logic device architecture;

configuring a selected system under test of said plurality of systems under test with ~~having~~ said circuit implemented in said programmable logic ~~with a circuit design~~ according to said configuration data of said test job by way of a test server;

coupling said test vectors to said selected system under test;

receiving an output comprising result vectors from said selected system under test; and

comparing said result vectors from said selected system under test to expected result vectors.

17. (Previously Presented) The method of claim 16 further comprising a step of generating said test vectors at said client computer.

18. (Original) The method of claim 16 further comprising a step of generating said test vectors and expected result vectors on an external device.

19. (Currently Amended) The method of claim 16 wherein said step of coupling said test vectors to [[a]] said selected system under test comprises coupling test vectors by way of a test server.

20. (Previously Presented) The method of claim 19 further comprising a step of coupling said result vectors to said client computer by way of said test server.

21. (Currently Amended) A method of verifying a semiconductor design by way of a server, said method comprising the steps of:

coupling a plurality of client computers to a test server, each said client computer storing a test job for testing the design of a programmable logic circuit, [[said]] each test job having test vectors and configuration data for [[said]] a

programmable logic circuit;

providing a plurality of systems under test, each system under test having a different programmable logic device architecture;

reconfiguring a programmable logic circuit of a selected system under test with a circuit design according to [[said]] configuration data of [[said]] a test job by way of [[said]] a test server;

coupling test vectors of a predetermined test job to said selected system under test by way of said test server;

receiving an output comprising result vectors from said selected system under test; and

comparing said result vectors from said selected system under test to expected result vectors.

22. (Currently Amended) The method of claim 21 further comprising a step of coupling [[a]] said plurality of systems under test to said test server.

23. (Original) The method of claim 21 further comprising a step of providing a test server having a network interface and a system under test interface.

24. (Original) The method of claim 23 further comprising a step of coupling said result vectors to said client computer by way of said test server.

25. (Currently Amended) The method of claim 21 wherein said step of comparing said result vectors from said selected system under test to expected result vectors comprises comparing said result vectors from said selected system under test to expected result vectors at said client computer.

26. (Currently Amended) A method of verifying a semiconductor design by way of a server, said method comprising the steps of:

coupling a plurality of client computers to a job distribution server, each said client computer storing a test job for testing the design of a programmable logic

circuit and having test vectors and configuration data for said programmable logic circuit;

providing a plurality of systems under test, each system under test having a different programmable logic device architecture;

reconfiguring a programmable logic circuit of a selected system under test of said plurality of systems under test with a circuit design according to [[said]] configuration data of [[said]] a test job received at said selected system under test by way of ~~said test~~ a job distribution server;

coupling said job distribution server to a plurality of servers, each said server coupling predetermined test vectors to a system under test of [[a]] said plurality of systems under test;

receiving an output comprising result vectors from [[a]] said selected system under test of said plurality of systems under test; and

comparing said result vectors from said selected system under test to expected result vectors.

27. (Previously Presented) The method of claim 26 further comprising a step of providing a first network between said plurality of client computers and said job distribution server.

28. (Original) The method of claim 27 further comprising a step of providing a second network between said plurality of servers and said job distribution server.

29. (Currently Amended) The method of claim 26 further comprising coupling [[a]] said plurality of systems under test to a server of said plurality of servers.

30. (Previously Presented) The method of claim 26 further comprising a step of coupling said output comprising result vectors to a client computer.